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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,714	08/25/2003	Muhammad Asif Khan	SETI-0002DIV	2476

7590 03/11/2004

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,714	KHAN ET AL.	
	Examiner	Art Unit	
	Thao P Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 24-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 24-29* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/25/03, 10/03/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Preliminary Amendment

1. Preliminary Amendment filed on 8/25/03 has been entered and made of record.

In Preliminary Amendment, applicant cancels claims 15-23, adds claims 24-29, and amends claims 1, 9, and 10. Accordingly, claims 1-14, 24-29 are pending in this application.

This application is a Divisional of the co-pending application serial number 09/966,559, filed on 09/27/01, which claims the benefit of U.S. provisional application serial number 60/235,563, filed on 09/27/00.

Oath/Declaration

2. The oath/declaration filed on 8/25/03 is acceptable.

Information Disclosure Statement

3. This office acknowledges of the following item from the Applicant:

The references cited on the PTOL 1449 forms of the Information Disclosure Statements (IDSs) filed on **8/25/03 and 10/03/03** have been considered.

Claim Objection

4. Claim 9 is objected to due to the following:

In claim 9, line 1, it appears that the word "contact" should be changed to --- contacts ---, "a source and a drain contact" in line 1 should be changed to either a) --- a source and a drain contacts ---, or b) --- a source contact and a drain contact ---.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) *A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

6. Claims 1-9, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheppard et al., U.S. Patent No. 6,486,502, and in view of Lipkin et al., U.S. Patent No. 6,246,076.

Regarding to claim 1, Sheppard et al. discloses a method of forming nitride based heterostructure devices similar to what recited in claim 1. See Fig. 1 and Cols. 1-10. Sheppard et al. discloses the method comprising the steps of:

. providing a substrate **11** (made of **SiC, Fig. 1, line 24, Col. 3**);

. applying a first layer **13 (Fig. 1)** over the substrate **11** wherein the first layer includes nitrogen (**GaN, lines 9-10, Col. 4**);

. applying a first contact **22** disposed above and adjoining to the first layer.

Sheppard et al. fails to disclose the steps of applying a dielectric layer over the first layer wherein the dielectric layer includes silicon dioxide, and applying the first contact 22 disposed above and adjoining to the dielectric layer instead of to the first layer.

However, Lipkin et al. (**See Figs. 2-4, Cols. 1-6**) discloses the method of forming high power, high field, or field effect transistors using silicon carbide as a substrate including the steps of applying a dielectric layer **21 (Fig. 2)** over stack layers and substrate wherein the dielectric layer includes silicon dioxide (**lines 29-30, Col. 4**), and applying a contact **22 (Fig. 2**) disposed above and adjoining the silicon dioxide dielectric layer **21 (See Fig. 2)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Sheppard et al. by forming a dielectric layer made of silicon dioxide under and adjoin the contact as taught in the method of Lipkin et al. **because** the silicon dioxide provides an excellent insulator with a wide band gap, thus, the silicon dioxide layer is an excellent barrier to prevent charge leaking **(Lipkin et al., lines 29-32, Col. 4),** thereby, prevent the reverse leakage of current. In

addition, silicon dioxide has low dielectric constant which makes it is more attractive for charge leaking prevention or current blocking in heterostructures.

Regarding to claim 2, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claim 1 above, and Sheppard et al. further discloses substrate 11 includes silicon carbide **(Fig. 1, line 24, Col. 3).**

Regarding to claim 3, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claim 1 above, and Sheppard et al. further discloses the first layer 13 includes a binary compound including one element of the group comprising group III element **(GaN, lines 9-10, Col. 4).**

Regarding to claims 4-5, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claim 1 above, and Sheppard et al, further discloses the first layer 13 includes a binary compound including one element of the group comprising group III element **(GaN, lines 9-10, Col. 4).** However, Sheppard et al. fails to disclose the first layer 13 includes a ternary compound including two elements of the group comprising group III elements (claim 4) or a quaternary compound including three elements of the group comprising group III elements (claim 5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use either binary compound including one element of group

comprising group III element, a ternary compound including two elements of the group comprising group III elements, or a quaternary compound including three elements of the group comprising group III elements **because** Sheppard et al. discloses that group III elements can combine with nitrogen to from binary (e.g. GaN), ternary (e.g. AlGaN), and quaternary (e.g. AlInGaN) compounds, and these compounds all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the group III elements (**lines 58-63, Col. 3**), and that either binary, ternary, or quaternary used as insulating layers in heterstructures would yield similar result whereas the device would have the same advantageous properties and characteristics (**lines 35-40**).

Regarding to claim 6, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claim 1 above, and Sheppard et al, further discloses the step of forming a second layer **14 (Fig. 1)** between the first layer 13 and the dielectric or contact wherein the second layer **14 (comprises three layers 15, 16, 17)** includes nitrogen (**lines 28-35, Col. 4**).

Regarding to claim 7, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claims 1 and 6 above, and Sheppard et al, further discloses wherein the first layer 13 includes a binary compound including one element of the group comprising group III element (**GaN, line 9-10, Col. 4**) and the second layer 14 further includes a ternary compound including two elements of the group comprising group III element (**AlGaN, lines 28-35, Col. 4**).

Regarding to claim 8, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claims 1 and 6 above, and Sheppard et al. further discloses the second layer 14 further includes a quaternary compound including three elements of the group comprising group III element (**AlInGaN, lines 35-39, Col. 4**). Sheppard et al. discloses the first layer 13 includes a binary compound including one element of the group comprising group III elements but fails to disclose the first layer 13 includes a ternary compound including two elements of the group comprising group III elements.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use either binary compound including one element of group comprising group III element, a ternary compound including two elements of the group comprising group III elements, or a quaternary compound including three elements of the group comprising group III elements **because** Sheppard et al. discloses that group III elements can combine with nitrogen to from binary (e.g. GaN), ternary (e.g. AlGaN), and quaternary (e.g. AlInGaN) compounds, and these compounds all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the group III elements (**lines 58-63, Col. 3**), and that either binary, ternary, or quaternary used as insulating layers in heterostructures would yield similar result whereas the device would have the same advantageous properties and characteristics (**lines 35-40**).

Regarding to claim 9, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claim 1 above, Sheppard et al. and Lipkin et al. further disclose the step of applying a source contact and a drain contact, and wherein the first contact is a gate contact **(Sheppard et al., gate 22, Fig. 1, lines 52-53, Col. 4), (Lipkin et al., gate 22, Fig. 2, line 28, Col. 4).**

Regarding to claim 24, Sheppard et al. and Lipkin et al. disclose the limitations as applied to claims 1 and 9 above, Sheppard et al. discloses the steps of forming a dielectric layer comprising silicon dioxide **23** material on the nitride layer **(23, Fig. 1, lines 45-46, Col. 5)** wherein the dielectric 23 further contacts the source contact 20 and the drain contact **21 (See Fig. 1)**.

7. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheppard et al., U.S. Patent No. 6,486,502, and in view of Lipkin et al., U.S. Patent No. 6,246,076.

Regarding to claim 10, Sheppard et al. discloses a method of forming nitride based heterostructure devices similar to what recited in claim 10. **See Fig. 1 and Cols. 1-10**. Sheppard et al. discloses the method comprising the steps of:

. providing a substrate **11** (made of **SiC, Fig. 1, line 24, Col. 3**);

. applying a first layer **13 (Fig. 1)** over the substrate **11** wherein the first layer includes **gallium and nitrogen (GaN, lines 9-10, Col. 4)**;

. applying a first contact **22** on the first layer.

Sheppard et al. fails to disclose the step of applying a dielectric layer over the first layer wherein the dielectric layer includes silicon dioxide and applying the first contact 22 on the dielectric layer.

However, Lipkin et al. (**See Figs. 2-4, Cols. 1-6**) discloses the method of forming high power, high field, or field effect transistors using silicon carbide as a substrate including the steps of applying a dielectric layer **21 (Fig. 2)** over stack layers and substrate wherein the dielectric layer includes silicon dioxide (**lines 29-30, Col. 4**), and applying a contact **22 (Fig. 2**) on the silicon dioxide dielectric layer **21**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Sheppard et al. by forming a dielectric layer made of silicon dioxide under the contact as taught in the method of Lipkin et al. **because** the silicon dioxide provides an excellent insulator with a wide band gap, thus, the silicon dioxide layer is an excellent barrier to prevent charge leaking **(Lipkin et al., lines 29-32, Col. 4),** thereby, prevent the reverse leakage of current. In addition, silicon dioxide has low dielectric constant which makes it is more attractive for charge leaking prevention or current blocking in heterostructures.

Regarding to claim 11, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claim 10 above, and Sheppard et al. further discloses substrate 11 includes silicon carbide (**Fig. 1, line 24, Col. 3).**

Regarding to claim 12, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claim 10 above, and Sheppard et al. further discloses the step of forming a second layer **14 (Fig. 1)** between the first layer 13 and the dielectric (or contact) wherein the second layer **14 (comprises three layers 15, 16, 17)** includes aluminum, gallium, and nitrogen (**AlGaN, lines 28-35, Col. 4**).

Regarding to claim 13, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claims 10 and 12 above, and Sheppard et al. further discloses substrate 11 includes silicon carbide (**Fig. 1, line 24, Col. 3).**

Regarding to claim 14, Sheppard et al. and Lipkin et al. disclose the claimed limitations as applied for claims 10 and 12 above, and Sheppard et al. further discloses the first layer includes aluminum **(GaN, lines 9-10, Col. 4)** and the second layer further includes indium **(InGaN or AlInGaN, lines 35-40, Col. 4).**

8. Claims 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over S.C. Binari et al., DC, Microwave, and High-Temperature Characteristics of GaN FET structures, Inst. Phys. Conf. Ser. No. 141: Chapter 4, Presented at Int.

Symp. Compound Semicond., San Diego, CA, Sep. 18-22, 1994, pp. 459-462 (Applicant submitted as prior art), and in view of Lipkin et al., U.S. Patent No. 6,246,076.

Regarding to claim 25, S.C. Binari et al. discloses a method of producing a nitride based heterostructure transistor similar to what recited in claim 25. S.C. Binari et al. discloses the method comprising the steps of:

. providing a substrate (**sapphire, Fig. 4**);

. applying a buffer layer **(40 nm AlN)** on the substrate, wherein the buffer layer includes aluminum and nitrogen **(AlN, Fig. 4);**

. applying an active layer (**GaN**) on the buffer layer, wherein the active layer includes gallium and nitrogen **(GaN, Fig. 4)**;

. applying a barrier layer on the active layer, wherein the barrier layer includes aluminum and nitrogen **(layers 6 nm AlN and 200 nm GaN, Fig. 4);**

. applying a dielectric layer (**silicon nitride**) on the barrier layer;

. applying a first contact **Al** on the dielectric layer (**Fig. 4**).

S.C. Binari et al. discloses the dielectric layer includes silicon nitride but fails to disclose the dielectric layer includes silicon dioxide.

However, Lipkin et al. (**See Figs. 2-4, Cols. 1-6**) discloses the method of forming high power, high field, or field effect transistors using silicon carbide as a substrate

including the step of forming a dielectric layer **21 (Fig. 2)** under a gate contact wherein the dielectric layer includes silicon dioxide (**lines 29-30, Col. 4**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of S.C. Binari et al. by using silicon dioxide material as the dielectric layer formed under the contact as taught in the method of Lipkin et al. **because** the silicon dioxide provides a better insulator with a wide band gap and has lower dielectric constant, thus, the silicon dioxide layer is a better barrier to prevent charge leaking **(Lipkin et al., lines 29-32, Col. 4)** compare to silicon nitride, thereby, a better layer to prevent the reverse leakage of current. Silicon dioxide has lower dielectric constant **(3.8~3.9 vs. 6~9 for CVD silicon nitride)** which makes silicon dioxide is more attractive for charge leaking prevention or current blocking in heterostructures. In addition, it is much easier to achieve uniform, thin, and controllable thickness of silicon dioxides at a much lower cost compare to silicon nitride, using thermal oxidation. A very thin silicon dioxide layer can be formed even at room temperature.

Regarding to claim 26, S.C. Binari et al. and Lipkin et al. disclose the claimed limitations as applied for claim 25, and S.C. Binari et al. further discloses at least a portion of the barrier layer remains uncovered by the dielectric layer (portions under the source/drain contacts) (Fig. 4).

Regarding to claim 27, S.C. Binari et al. and Lipkin et al. disclose the claimed limitations as applied for claims 25 and 26 above, S.C. Binari et al. further discloses the steps of forming a source contact and a drain contact on the barrier layer and wherein the first contact on the dielectric layer comprises a gate contact (Fig. 4).

Regarding to claim 28, S.C. Binari et al. and Lipkin et al. disclose the claimed limitations as applied for claims 25, 26, and 27 above, S.C. Binari et al. further discloses wherein the dielectric layer further contacts the source and drain contacts (**see Fig. 4**).

9. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over S.C. Binari et al., DC, Microwave, and Hing-Temperature Characteristics of GaN FET structures, Inst. Phys. Conf. Ser. No. 141: Chapter 4, Presented at Int. Symp. Compound Semicond., San Diego, CA, Sep. 18-22, 1994, pp. 459-462 (Applicant submitted as prior art), and in view of Lipkin et al., U.S. Patent No. 6,246,076, and further in view of Sheppard et al., U.S. Patent No. 6,486,502.

Regarding to claim 29, S.C, Binari et al. and Lipkin et al. discloses the claimed limitations as applied for claim 25 above but fail to disclose wherein the active layer comprises an insulating layer and an n-type layer on the insulating layer.

However, Sheppard et al. discloses the method of forming nitride based transistor including the step of forming an active layer 14 comprises an insulating layer

15 (undoped AlGaN) and an n-type layer 16 (n-doped layer AlGaN) on the insulating layer 15.

It would have been obvious to one having skill in the art at the time the invention was made to form the active layer comprising an insulating layer and an n-type layer as taught by Sheppard et al. in Binari et al. and Lipkin et al.'s methods **because** n-type doing layer formed on the insulating layer increases capacitance, increases current density, and yet lowers parasitic capacitances and lowers device resistances.

10. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

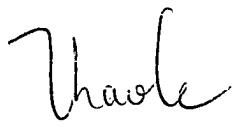
A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **David Nelms** can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao P. Le